What is claimed is:

1. A substrate for forming a ball grid array (BGA) package, comprising:

a substrate having a top surface and a bottom surface, the bottom surface having ball pads; and

a plurality of enhanced pads formed on the bottom surface, each enhanced pad having one or more dummy pads coupled to one or more dummy patterns.

2. The substrate of claim 1, wherein said enhanced pads are formed near an outer edge of said substrate.

3. The substrate of claim 2, further comprising a solder ball formed on said ball pad.

4. A semiconductor chip package comprising:

a substrate having a top surface and a bottom surface, the bottom surface having ball pads;

a plurality of enhanced pads formed on the bottom surface, each enhanced having one or more dummy pads coupled to one or more dummy patterns;

a semiconductor chip mounted on and electrically connected to the top surface of the substrate.

5. The semiconductor chip package according to claim 4, wherein said enhanced pads are formed near an outer edge of said substrate.

6. The semiconductor chip package according to claim 4, further comprising a molding resin for encapsulating said semiconductor chip.

7. The semiconductor chip package according to claim 4, further comprising solder balls formed on said ball pads.

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9. The semiconductor chip package according to claim 1, wherein said enhanced pads comprise a first enhanced pad, and wherein the first enhanced pad comprises a ball pad, a plurality of dummy pads, and a plurality of dummy patterns configured to connect said ball pad to said dummy pads.

10. The semiconductor chip package according to claim 9, wherein the first enhanced pad comprises two dummy pads and two dummy patterns.

11. The semiconductor chip package according to claim 10, said two dummy pads are arranged perpendicular to each other.

12. The semiconductor chip package according to claim 1, wherein said enhanced pads comprise a second enhanced pad, and wherein the second enhanced pad comprises a ball pad, a dummy pad, and a dummy pattern connecting said ball pad to said dummy pad.

13. The semiconductor chip package according to claim 1, wherein said enhanced pads comprise a third enhanced pad, and wherein the third enhanced pad comprises a plurality of dummy pads and a dummy pattern for connecting said dummy pads to each other.

14. The semiconductor chip package according to claim 1, further comprising a board, said board comprising enhanced lands corresponding to said enhanced pads and ball lands corresponding to said ball pads, wherein said semiconductor chip package is mounted on said board.

15. The semiconductor chip package according to claim 14, wherein said semiconductor chip package is mounted on said board by attaching said solder balls formed on said ball pads and said dummy pads of said package to a solder paste coated on said ball lands and said enhanced lands of said board.

16. The semiconductor chip package according to claim 15, wherein said solder paste is uniformly formed on said solder balls and said dummy patterns of the enhanced pads by a solder reflow process.

17. The semiconductor chip package according to claim 1, wherein said solder balls are all approximately the same size.

18. The semiconductor chip package according to claim 1, wherein a majority of said dummy patterns are arranged parallel to a long side of said substrate.

19. A method of forming a substrate for a BGA package, comprising:

arranging ball pads on a bottom surface of the substrate;

arranging a plurality of enhanced pads on the bottom surface of the substrate, said enhanced pads comprising at least one dummy pad coupled to at least one dummy pattern.

20. The method according to claim 19, wherein arranging said enhanced pads further comprises arranging said enhanced pads near sides of the substrate.

21. The method according to claim 19, further comprising arranging a majority of the dummy patterns parallel to a long side of the substrate.

22. The method according to claim 19, wherein one or more of said enhanced pads comprise a plurality of dummy patterns.

23 24. The method of attaching a semiconductor package to a board, comprising:

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preparing a board by exposing ball lands and enhanced lands from a photo solder resist (PSR) layer;

applying a mask, having openings corresponding to the ball lands and the enhanced lands, to the board;

applying a solder paste on the ball lands and the enhanced lands;

removing the mask;

attaching solder balls to ball pads and enhanced pads of a substrate; and

attaching the substrate to the board with the solder balls and the solder paste using a solder reflow process,

wherein each of said enhanced pads comprises one or more dummy pads coupled to one or more dummy patterns.

25. A method according to claim 24, wherein an external connection terminal is formed over an entire area of the enhanced pad.

26. A method according to claim 24, wherein each of said ball lands corresponds to one of the ball pads and wherein each of the enhanced lands corresponds to one of the enhanced pads.